REMARKS

Reconsideration and allowance of the above referenced application are respectfully requested.

Initially, the indication that claims 3-8, 14-16, 22-30, 35-36, 39-45, 47, 50-54, 89-91, 96-105, 107-110 and 115-117 are allowed is appreciatively noted. All of these claims are retained. In addition, claims 3, 26, 29, 35, 43, 44, 96, 101, 115 and 117 have been amended into allowable independent form. Each of these allowable claims, whether rewritten into independent form or not, should remain in condition for allowance.

Claims 1-2, 9-10, 11-13, 17-19, 20-21, 31-34, 37-38, 46, 48-49, 86-88, 92-95, 106, 111-114 and 135 stand rejected under 35 USC 102b as allegedly being anticipated by U.S. patent No. 5,883,830 to Hirt, henceforth '830. This contention is respectfully traversed, and for reasons set forth herein, it is respectfully suggested that the rejection does not meet the patent office's burden of providing a prima facie showing of unpatentability.

Claim 1 recites a substrate having integrated thereon both an image acquisition portion and a control portion. The image acquisition portion includes active pixel type photoreceptors

with both a photoreceptor and a readout amplifier in the same substrate. The control portion is recited to include a signal controlling device that controls the photoreceptors to output their signals, and a timing circuit that controls the timing of operation of the photoreceptors. It is respectfully suggested that this claimed structure is not taught or suggested by '830.

Admittedly, '830 teaches the use of an active pixel photodetection element.

The rejection states that the control portion reads on control unit 16. However, the control unit 16 in '830 is a controller which "calculates compensation values", see for example column 5 line 12. The controller in '830 controls interaction with the flash programming unit that stores compensation values. As '830 explains with reference to figure 2 and beginning at column 5 line 47, the controller 16 calculates the compensation values for each of the pixels. The memory is flash programmed, and then the sensor array is illuminated. The controller may adjust the individual signals from the sensor array using the compensation values, see column 5, lines 58-60. It is respectfully suggested that 830 does not teach that the controller controls the photoreceptors to output their signals as claimed, nor control the timing of operation of the array of photoreceptors as claimed. '830 only teaches that

the controller controls compensation of the pixel values. Therefore, the rejection does not meet the patent office's burden of providing a prima facie showing of unpatentability. Nowhere does '830 teach or suggest that the on-substrate controller controls the photoreceptors to output their signals, and controls timing of the operation of the array of photoreceptors. Since '830 does not teach or suggest this operation being done on-chip, presumably all of this is done off chip.

Claim 1 should therefore be allowable.

The rejection alleges that a timing circuit is inherently included in the device, since the circuit is used to control signal readout operation; see page 3 of the official action. However, it is respectfully suggested that this is based on hindsight and not on '830's teaching. A timing circuit could very easily have been incorporated off chip, so that the operation was controlled through the I/O port 22. In fact, 830 does not teach a timing circuit on chip, and therefore presumably one would assume that all of this information was calculated and received from off chip. All that '830 teaches is compensating the values on chip. There is no teaching of doing the timing using an on chip timing circuit, as claimed.

Claim 2 should be allowable for similar reasons. Nowhere

is there any teaching or suggestion that an entire row of photoreceptors is output substantially simultaneously as claimed.

Claims 9-10 should be allowable for similar reasons to those discussed above with respect to claim 1.

Claim 11 similarly defines a control portion that controls the photoreceptors to output their signals "in a way such that at least a plurality of said photoreceptors output their signals at substantially the same time". Again, as described above, the controller in '830 is only described as controlling compensation values. Nowhere does '830 teach or suggest that a plurality of the photoreceptors output their signals at substantially the same time. In fact, the flowchart of figure 2 at least implies that the signals are analyzed one by one. This therefore might imply that the signals may be output one by one. In any case, '830 does not teach or suggest outputting the signals at substantially the same time, as claimed.

As noted above, '830 also does not teach the control portion including a timing circuit that controls timing of operation. Any contention to the contrary is entirely based on hindsight. Therefore, it is respectfully suggested that the rejection does not meet the patent office's burden of providing a prima facie showing of unpatentability.

Claim 12 defines a column parallel readout device reading an entire row of photoreceptors at the same time. As described above, nothing in 830 teaches or suggests such a device. In fact, '830 may appear to intend that the pixels be read out one by one. In any case, there is no teaching or suggestion of such a device in '830. Therefore, it is respectfully suggested that the patent office has not met their burden of providing a prima facie showing of unpatentability for claim 12.

Claim 13 defines a column selector that selects a column for readout and a row selector that selects a row for readout. While admittedly there are column and row selection signals in the '830 circuit, nowhere is there any teaching or suggestion that the column selector is carried out on-chip. This is not inherent, since the selection may be generated off-chip. Accordingly, the rejection does not meet the patent office's burden of providing a prima facie showing of unpatentability. The remaining dependant claims should be allowable for similar reasons to those discussed above with respect to the respective independent claims.

Claim 31 should be allowable for analogous reasons. Claim 31 defines that the control portion includes "a preset buffer, allowing preset of at least one of a start address for an output or a stop address for output". It is respectfully suggested

that there is absolutely nothing in '830 which teaches or suggests such a preset buffer in the control portion. Therefore, claim 31 should be even further allowable in addition to the reasons discussed above. Claim 31 also recites a timing circuit that controls timing of operation and again this should be allowable. Claims 32-33 should be allowable for reasons discussed above with respect to the other dependent claims which have analogous limitations.

Claim 34 specifies values on a data bus being used for preset of start and stop values. Again, there is nothing teaching or suggesting this in the cited prior art.

The remaining dependent claims should be allowable for analogous reasons.

Claim 46 defines that the control portion controls a timing in either a first mode or a second mode depending on the type of photoreceptor which is being used. '830 clearly does teach that different kinds of photoreceptors can be used. However, there is no teaching or suggestion that the control portion controls the timing based on which type of photoreceptor is being used. For these reasons, the rejection using 830 does not meet the patent office's burden of providing a prima facie showing of unpatentability of these claims.

The remaining dependant claims should be allowable for

similar reasons to those discussed above with respect to the respective independent claims.

Claim 86 should be allowable for reasons discussed above and specifically based on the control portion which controls the photoreceptors to output their signals and the timing circuit controlling a timing of operation of the array of photoreceptors. As described above, this is not taught or suggested by '830. In addition, however, claim 86 defines that the control portion includes "common logic elements to control row and address decoders and delay counters. Nowhere does' 830 in any way teach or suggest on-chip row and address decoders and delay counters. Claims 87-88 should be allowable for similar reasons to those discussed above with respect to claims which include analogous limitations. The remaining dependent claims should be similarly allowable for similar reasons discussed above with respect to the independent claim.

Claim 106 similarly recites a control portion with a signal controlling device and a timing circuit. As discussed above, this is in no way taught or suggested by '830. Claim 106 also defines that the control portion includes "common logic elements to control all pixels on the selected row to sample said all pixels onto said charge storage elements substantially simultaneously." This is not taught or suggested by '830.

Nothing in '830 teaches sampling all pixels in a selected row substantially simultaneously. In fact, as described above, '830 appears to imply that pixels should be sampled at individual times, not simultaneously.

The remaining dependant claims should be allowable for similar reasons to those discussed above with respect to the independent claims. Claim 135 specifies a method of control where an image acquisition portion and a control portion are integrated on a single substrate. A first mode of operation is established by the on-chip circuitry when the photoreceptors are photogates. A second mode of operation is established by the on-chip circuitry when the photoreceptors are photodiodes. The timing for the first mode is different than a timing for the second mode. Nowhere is there any teaching or suggestion of this structure in '830. In fact, it is respectfully suggested that nothing in '830 teaches or suggests using the on-chip circuits to control timing of rows at all, much less in the way claimed. Specifically, claim 135 defines using on chip circuits to operate in a first sequence for photogates and in a second mode of operation for photodiodes with different timings for the two modes. Nothing in the cited prior art is in any way suggestive of this operation, and therefore it is respectfully suggested that the rejection does not meet the patent office's

burden of providing a prima facie showing of unpatentability.

In view of the above amendments and remarks, it is respectfully suggested that all of the claims should be in condition for allowance. A notice of allowance is respectfully solicited.

Enclosed is a $924.00 check for excess claim fees. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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Attached is a marked-up version of the changes being made by the current amendment.